

FORM PTO-1449
INFORMATION DISCLOSURE
STATEMENT BY APPLICANT(S)

Atty Docket No.: 29287/141
 Serial No.: ~~To be assigned~~ 10/765923
 Inventors: Hiroyuki MIZUNO et al.
 Filed: January 29, 2004
 Group Art Unit: 2816 (anticipated)
 Examiner: J.S. Zweizig (anticipated)

U.S. PATENT DOCUMENTS

Examiner Initial	Patent Number	Patent Date	Name	Class/ Subclass	Filing Date
JZ	6,380,798	04-2002	MIZUNO et al.	327/534	
JZ	6,337,593	01-2002	MIZUNO et al.	327/534	
JZ	6,292,015	09-2001	OOISHI et al.	326/33	
JZ	6,191,615	Feb. 2001	KOGA	326/81	
JZ	6,177,831	Jan. 2001	YONEDA et al.	327/537	
JZ	6,097,113	Aug. 2000	TERAOKA et al.	307/125	
JZ	6,046,627	04-2000	ITOH et al.	327/546	
JZ	5,786,724	Jul. 1998	TEGGATZ	327/534	
JZ	5,659,517	08/19/97	ARIMOTO et al.	365/226	
JZ	5,610,533	Mar. 1997	ARIMOTO et al.	326/33	
JZ	5,721,510	02-1998	MIYAJIMA	327/536	
JZ	4,628,215	12/09/86	LOU	307/200	

FOREIGN PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Country	Class/ Subclass	Translation Yes No
JZ	JP7-254685	10/3/95	Japan		
JZ	JP8-83487	3/26/96	Japan		
JZ	JP8-204140	8/09/96	Japan		
JZ	06-053496	02/25/94	Japan		
JZ	60-020550	02/01/85	Japan		
JZ	01-098254	04/17/89	Japan		
JZ	08-249882	09/27/96	Japan		
JZ	01-318261	12/22/89	Japan		
JZ	04-345061	12/01/92	Japan		
JZ	05-190672	07/30/93	Japan		
JZ	02-154446	06/13/90	Japan		

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Jeffrey Zweizig

DATE CONSIDERED

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OTHER DOCUMENTS

(Including Author, Title, Date, Pertinent Pages, Etc.)

Examiner
Initial

- | | | |
|-----------|----|---|
| <u>JZ</u> | 1. | Kiyoo Ito, "VLSI Memory" p. 266, published by Baifukan |
| <u>JZ</u> | 2. | Soden et al., "Identifying Defects in Deep-Submicron CMOS lcs",
September 1996, pp. 66-71, IEEE SPECTRUM |
| <u>JZ</u> | 3. | Mizuno et al., "A Lean-Power Gigascale LSI Using Hierarchical VBB
Routing Scheme with Frequency Adaptive VT CMOS", 1997, pp. 95-
96, Symposium on VLS Circuits Digest of Technical Papers |

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